Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method of managing ~~queue entries~~ queues comprising:

storing addresses corresponding to ~~one of~~ a plurality of data buffers having a corresponding number of cells in a ~~first~~ queue ~~entry~~ configured as a ~~circular~~ linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, wherein ~~the~~ a first BDA entry points to a subsequent BDA entry and to a final BDA entry, each of the plurality of BDA entries of the ~~circular~~ linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer;

retrieving a first address from the ~~first~~ queue ~~entry~~; and

modifying the linked list of addresses of the ~~first~~ queue ~~entry~~ based on the cell count of the first address retrieved, including decrementing the cell count of the first address each time the first address is retrieved.

2. (Cancelled)

3. (Previously presented) The method of claim 1, further comprising:

determining the cell count is zero.

4. (Currently amended) The method of claim 3, wherein storing addresses further comprises:

setting the first address as the head address of the ~~first~~ queue ~~entry~~; and

linking a second address to the first address of the ~~first~~ queue ~~entry~~.

5. (Currently amended) The method of claim 4, wherein linking the second address to the first address further comprises:

setting the second address as a tail address of the ~~first~~ queue ~~entry~~.

6. (Currently amended) The method of claim 5, further comprising:

linking a third address to the ~~first~~ queue ~~entry~~ by storing the third address in the location indicated by the tail address.

7. (Currently amended) The method of claim 5, further comprising:

incrementing a queue count indicating the number of BDA entries included in the queue ~~entry~~ each time an address is linked to the ~~first~~ queue ~~entry~~.

8. (Currently amended) The method of claim 4, wherein the ~~first~~ queue ~~entry~~ is stored as part of a queue array having a plurality of linked queues ~~queue entries~~.

9. (Currently amended) An article comprising a machine-readable medium that stores machine-executable instructions for managing a queue array, the instructions causing a machine to:

store addresses corresponding to ~~one of~~ a plurality of data buffers having a corresponding number of cells in a ~~first~~ queue ~~entry~~ configured as a ~~circular~~ linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, wherein ~~the~~ a first BDA entry points to a subsequent BDA entry and to a final BDA entry, each of the plurality of BDA entries of the ~~circular~~ linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer;

retrieve a first address from the ~~first~~ queue ~~entry~~; and

modify the linked list of addresses of the ~~first~~ queue ~~entry~~ based on the cell count of the first address retrieved, including decrementing the cell count of the first address each time the first address is retrieved.

10. (Cancelled)

11. (Previously presented) The article of claim 9, further comprising instructions causing a machine to:

determine the cell count is zero.

12. (Currently amended) The article of claim 11, wherein storing further comprises instructions causing a machine to:

set the first address as the head address of the ~~first~~ queue ~~entry~~; and

link a second address to the first address of the ~~first~~ queue ~~entry~~.

13. (Currently amended) The article of claim 12, wherein linking comprises setting the second address as a tail address of the ~~first~~ queue ~~entry~~.

14. (Currently amended) The article of claim 13, further comprising instructions causing a machine to:

link a third address to the ~~first~~ queue ~~entry~~ by storing the third address in the location indicated by the tail address.

15. (Currently amended) The article of claim 13, further comprising instructions causing a machine to:

increment a queue count indicating the number of BDA entries included in the queue ~~entry~~ each time an address is linked to the ~~first~~ queue ~~entry~~.

16. (Currently amended) The article of claim 12, wherein the ~~first~~ queue ~~entry~~ is stored as part of a queue array having a plurality of linked queues ~~queue entries~~.

17. (Currently amended) An apparatus, comprising:

a first storage device for holding queues ~~queue entries~~;

a second storage device for holding data packets;

a memory that stores executable instructions; and

a processor that executes the instructions to:

store addresses corresponding to ~~one of~~ a plurality of data buffers having a corresponding number of cells in a ~~first~~ queue ~~entry~~ configured as a ~~circular~~ linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, wherein ~~the~~ a first BDA entry points to a subsequent BDA entry and to a final BDA entry, each of the plurality of BDA entries of the ~~circular~~ linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer;

retrieve a first address from the ~~first~~ queue ~~entry~~, and

modify the linked list of addresses of the ~~first~~ queue ~~entry~~ based on the cell count of the first address retrieved, including decrementing the cell count of the first address each time the first address is retrieved.

18. (Cancelled)

19. (Previously presented) The apparatus of claim 17, wherein instructions to modify comprise instructions to:

determine the cell count is zero.

20. (Currently amended) The apparatus of claim 19, wherein instructions to store addresses comprises instructions to:

set the first address as the head address of the ~~first~~ queue ~~entry~~; and

link a second address to the first address of the ~~first~~ queue ~~entry~~.

21. (Currently amended) The apparatus of claim 20, wherein instructions to link comprises instructions to:

set the second address as a tail address of the ~~first~~ queue ~~entry~~.

22. (Currently amended) The apparatus of claim 21, further comprising instructions to:

link a third address to the ~~first~~ queue ~~entry~~ by storing the third address in the location indicated by the tail address.

23. (Currently amended) The apparatus of claim 21, further comprising instructions to:

increment a queue count indicating the number of BDA entries included in the queue ~~entry~~ each time an address is linked to the ~~first~~ queue ~~entry~~.

24. (Currently amended) The apparatus of claim 20, further comprising:

a storage medium, the ~~first~~ queue ~~entry~~ being stored on the storage medium as part of a queue array having a plurality of linked queues ~~queue entries~~.

25. (Currently amended) A processing system for managing queues ~~queue entries~~ comprising:

a processor;

a memory to store queues ~~queue entries~~; and

a storage-medium accessible by the processor to store executable instructions, which when accessed by the processor ~~causes~~ cause the processor to:

store addresses corresponding to ~~one of~~ a plurality of data buffers having a corresponding number of cells in a ~~first~~ queue ~~entry~~ configured as a ~~circular~~ linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, wherein ~~the~~ a first BDA entry points to a subsequent BDA entry and to a final BDA entry, each of the plurality of BDA entries of the ~~circular~~ linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer;

retrieve a first address from the ~~first~~ queue ~~entry~~; and

modify the linked list of addresses of the ~~first~~ queue ~~entry~~ based on the cell count of the first address retrieved, including decrementing the cell count of the first address each time the first address is retrieved.

26. (Cancelled)

27. (Currently amended) The ~~method~~ system of claim 25, further comprising instructions, which when accessed by the processor causes the processor to:

determine the cell count is zero.

28. (Currently amended) The system of claim 27, wherein storing addresses further comprises:

setting the first address as the head address of the ~~first~~ queue ~~entry~~; and

linking a second address to the first address of the ~~first~~ queue ~~entry~~.

29. (Currently amended) The system of claim 28, wherein linking the second address to the first address further comprises instructions, which when accessed by the processor causes the processor to:

setting the second address as a tail address of the ~~first~~ queue ~~entry~~.

30. (Currently amended) The system of claim 29, further comprises instructions, which when accessed by the processor causes the processor to:

link a third address to the ~~first~~ queue ~~entry~~ by storing the third address in the location indicated by the tail address.

31. (Currently amended) The system of claim 29, further comprises instructions, which when accessed by the processor causes the processor to:

increment a queue count indicating the number of BDA entries in the queue ~~entry~~ each time an address is linked to the ~~first~~ queue ~~entry~~.

32. (New) The method of claim 1, further comprising:

receiving network packets; and

storing the packets in one or more of the plurality of data buffers.

33. (New) The article of claim 9 further comprising instructions that cause the machine to:

receive network packets; and

store the packets in one or more of the plurality of data buffers.

34. (New) The apparatus of claim 17, wherein the processor executes further instructions to:

receive network packets; and

store the packets in one or more of the plurality of data buffers.

35. (New) The processing system of claim 25, wherein the storage medium further includes instructions that when accessed by the processor cause the processor to:

receive network packets; and

store the packets in one or more of the plurality of data buffers.